ISC1308
1280 x 1024, 12 µm
Two Color ROIC

Specification and Requirements

February 3, 2015

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Document Revision History

- **Version 1.00, May 9, 2013**
  - Initial Release
- **Version 1.01, February 3, 2015**
  - Updated specification tables to agree with final document

ISC1308 Specification and Requirements Review (1 of 5)

ROIC PARAMETER	SPECIFICATION REQUIREMENT	COMMENTS
Array Configuration	1280 x 1024	
Pixel Pitch	12 µm	
Input Polarity	Selectable P-on-N (Current Flows into Inputs) & N-on-P (Current Flows out of Inputs)	Color selectable on a per frame basis SLS, InSb, HgCdTe, QWIP One color operation only if detector biased externally.
Detector Interface	5 x 5 array of metal filled vias per pixel plus detector common pad ring around cell array. Planar top	One indium bump connection per pixel. 2 pixel wide ring of dummy pixels around active array. 4 pixel wide ring of shorted pixels around dummy pixels. Total array size is 1292 x 1036.
Test Detector Pads	4 pads to test individual detectors	
Input Configuration	Direct Injection (DI)	
Detector Impedance (R_RA_D) at 77 K	> $1.0x10^3$ (Ohm-cm^2)	Reverse bias impedance. Used for performance analysis, prediction and simulation
Detector Capacitance	≤ 100 fF	Used for performance analysis, prediction and simulation
Temperature Of Operation	65 K – 300 K	Specs defined for 77 K. Room temperature operation will have reduced performance.

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ROIC PARAMETER	SPECIFICATION REQUIREMENT	COMMENTS
Input Biases	VDETCOM -0.7 V to +4.3 V VPOS 3.6 V VPOSOUT 3.6 V VPOSD 3.6 V VPD 1.8 V VNEG 0.0 V VNEGOUT 0.0 V VND 0.0 V VOUTREF 1.1 V to 3.3 V	Detector Common Analog Positive Output Positive Digital Positive Digital Positive Analog Negative Output Negative Digital Negative Analog Reference, P-on-N = 1.1 V, N-on-P = 3.3 V
Input Clocks	Name Vhigh to Vlow CLK VPD to VND LSYNC VPD to VND FSYNC VPD to VND DATA VPD to VND RESET_B VPD to VND	 Master Clock Line Sync Frame Sync (Integ. Control) Mode Control Master Reset (optional)
Input Clock Rise and Fall	10% to 90% in 10 ns	
Outputs	Selectable 4, 8 or 16 with Reference Output	
Output Interface	≥ 100 kOhms ≤ 12 pF	12 pF includes capacitive load up to and including wire-bond to ROIC pad

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ROIC PARAMETER	SPECIFICATION REQUIREMENT	COMMENTS
Output Voltage Swing	2.1 V ± 0.2 V (Baseline P-on-N ~1.1 V ± 0.1 V) (Baseline N-on-P ~3.3 V ± 0.1 V)	Default settings: ~2.1 V typical output range at 77 K Estimated range for 0.2 V reverse bias. Output swing dependent on reverse bias.
Power (Full frame, T = 77 K)	4 outputs ≤ 120 mW 8 outputs ≤ 140 mW 16 outputs ≤ 190 mW	11.11 MHz clock rate
Programmable Test	Test Row Input Unit Cell Test Injection	
Detector Bias Adjust (P on N)	< 0 mV to > 800 mV reverse bias adjustment @ nominal current (1 nA)	~8.5-9 mV bias control per color
Detector Bias Adjust (N on P)	< 0 mV to > 800 mV reverse bias adjustment @ nominal current (1 nA)	~8.5-9 mV bias control per color
Large Detector Bias	Extra 0.7 V of detector reverse bias (Total reverse detector bias of > 1.5 V)	External VDETCOM supply required and run in only one color mode

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ROIC PARAMETER	SPECIFICATION REQUIREMENT	COMMENTS
Integration Mode	Snapshot ITR and IWR	Integrate one color per frame
Integration Time	100 µs to 0.9*full frame Adjustable on a per frame basis	Tint programmable to < 1 µs, but non-linear behavior expected for Tint < 100 µs.
Total Input Current Min Nominal Max	 20 pA 1 nA 50 nA	Simulation Range, includes signal and dark current
Input Charge Handling	≥ 10 x 10^6 carriers	GAIN = 0: > 3.0 x 10^6 GAIN = 1: > 11.5 x 10^6 Operating at 0.2 V reverse bias with detector bias set on-chip
Charge Handling Gain Adjustment	Per frame adjustability of charge capacity	Reduce input charge handling by 4x through the control word
Non-Linearity	< ± 0.5% from least squares line fit	Output Voltage vs. Tint Max Dev. from least squares fit over 10% to 90% of full range
Noise	≤ -78 dB of Full Well (Input Referred) At Maximum Readout Rate	Without Detector or System Noise. ROIC noise in dB defined as 20*log (noise e- / full well e-)

ISC1308 Specification and Requirements Review (5 of 5)

ROIC PARAMETER	SPECIFICATION REQUIREMENT	COMMENTS
Invert / Revert	Reverse Order Of Rows / Columns	Select Using Control Register
Temperature Sensor	0.75 V ± 0.05 V @ 300 K 1.07 V ± 0.05 V at 77 K	Temp Pad
Full Frame Rate (Pixel Rate 22.2 MHz and T = 77 K)	4 Output ≥ 60 FPS 8 Output ≥ 105 FPS 16 Output ≥ 180 FPS	4 Output 1280 x 720 ≥ 80 FPS 8 Output 1280 x 720 ≥ 150 FPS 16 Output 1280 x 720 ≥ 240 FPS
Data Valid / Settling Time	Settle to 0.1% @ T=77 K in ≤ 35 ns	12 pF // 100 kΩ load Default power settings
Adjacent ROIC Pixel Crosstalk	< 0.15% @ T=77 K < 0.15% @ T=300 K	
Non-Adjacent ROIC Pixel Crosstalk	< 0.1% @ T=77 K < 0.3% @ T=300 K	Limited routing and system impedance, depends on signal
Color-Color ROIC Pixel Crosstalk	< 0.15% @ T=77 K < 0.15% @ T=300 K	
Minimum Window Size and Resolution	≤ 16 columns x 4 rows ≤ 32 columns x 4 rows ≤ 64 columns x 4 rows	4 Output Mode 8 Output Mode 16 Output Mode
Die Size	19.0 mm x 17.5 mm - Optical center to lower edge ≤ 11.18 mm - All circuitry/pads in 26 mm circle centered at optical center - First active pixel to bond pad edge ≤ 1 mm	To edge of scribe lane