TELEDYNE FLIR
Everywhere**you**look™

**ISC1902
2048 x 2048, 10 µm
Large Well ROIC**

Specification and Requirements

October 5, 2021

Document Revision History

- **Version 1.00, August 20, 2019**
  - Initial Release

- **Version 1.10, October 5, 2021**
  - Update to markings and logos
  - Add clarification what SFA stands for

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ROIC PARAMETER	SPECIFICATION REQUIREMENT	COMMENTS
Array Configuration	2048 x 2048	
Pixel Pitch	10 µm	
Input Polarity	P-on-N (Current Flows into Inputs)	SLS, InSb, HgCdTe, QWIP
Detector Interface	Array of metal filled vias per pixel plus detector common pad ring around cell array. Planar top	One indium bump connection per pixel. 2 pixel wide ring of dummy pixels around active array. 4 pixel wide ring of shorted pixels around dummy pixels. Total array size is 2060 x 2060.
Test Detector Pads	4 pads to test individual detectors	
Input Configuration	Direct Injection (DI)	
Detector Impedance ($R_R A_D$) at 77 K	> 1.0x10^3 (Ohm-cm^2)	Reverse bias impedance. Used for performance analysis, prediction and simulation
Detector Capacitance	≤ 100 fF	Used for performance analysis, prediction and simulation
Temperature Of Operation	65 K – 300 K	Specs defined for 77 K. Room temperature operation will have reduced performance.

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ROIC PARAMETER	SPECIFICATION REQUIREMENT	COMMENTS
Input Biases	VDETCOM 3.6 V to 4.9 V VPOS 3.6 V VPOSOUT 3.6 V VPOSD 3.6 V VPD 1.8 V VNEG 0.0 V VNEGOUT 0.0 V VND 0.0 V VOUTREF 1.4 V to 3.3 V	Detector Common Analog Positive Output Positive Digital Positive Digital Positive Analog Negative Output Negative Digital Negative Analog Reference
Input Clocks	Name Vhigh to Vlow CLK VPD to VND LSYNC VPD to VND FSYNC VPD to VND INT VPD to VND DATA VPD to VND RESET_B VPD to VND	Master Clock Line Sync Frame Sync Integration Control Mode Control Master Reset (optional)
Input Clock Rise and Fall	10% to 90% in 10 ns	
Outputs	Selectable 8 or 16 Analog Outputs with Reference Outputs	16 Outputs: 0,1 Reference 8 Outputs: 0,1,2,4 References
Output Interface	≥ 100 kOhms ≤ 12 pF	12 pF includes capacitive load up to and including wire-bond to ROIC pad

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ROIC PARAMETER	SPECIFICATION REQUIREMENT	COMMENTS
Output Voltage Swing	1.6 V ± 0.1 V (Non-SFA) 1.5 V ± 0.1 V (Sub-Frame Avg) (Reset level ~1.5 V ± 0.1 V)	Default settings: ~1.6 V typical output range at 77 K Swing reduced ~100 mV for SFA
Power (Full frame, T = 77 K)	8 outputs ≤ 200 mW 16 outputs ≤ 250 mW	11.11 MHz clock rate
Programmable Test	Test Row Input Unit Cell Test Injection	
Detector Bias Adjust	< 0 mV to > 1100 mV reverse bias adjustment @ nominal current (1 nA)	~5.5 mV bias control 200 mV nominal reverse bias
Large Detector Bias	2.2 V reverse bias for QWIP applications	Requires VDETCOM at 4.9 V Maximum bias may degrade ROIC dynamic range, effective well capacity, and signal swing
Binning	2 x 2 Binning Mode	

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ROIC PARAMETER	SPECIFICATION REQUIREMENT	COMMENTS
Integration Mode	**Single Sample or Sub-Frame Avg (SFA) Snapshot ITR and IWR**	
Integration Time (per integration)	**20 µs to 16 ms Adjustable on a per integration basis**	**Tint programmable to < 1 µs**

Total Input Current
   Min
   Nominal
   Max
	20 pA
	1 nA
	35 nA
		Simulation Range, includes background, signal and dark current

Non-Linearity	**< ± 2.0% from least squares line fit**	**Output Voltage vs. Tint Max Dev. from least squares fit over 10% to 90% of full range**

Input Charge Handling	**Sub-Frame Avg (SFA):**
	   $\geq 19 \times 10^6$ effective carriers
	Single Sample:
	   $\geq 3 \times 10^6$ carriers
		Operating at 0.2 V reverse bias Effective carriers = Carriers in 1 sample * SFA_SNR_improvement^2

ROIC Dynamic Range	**$\leq$ -78 dB of Full Well (Input Referred) At Maximum Readout Rate Single Sample Mode**	**Without Detector or System Noise. ROIC noise in dB defined as 20*log (noise e- / full well e-)**

ROIC PARAMETER	SPECIFICATION REQUIREMENT	COMMENTS
Invert / Revert	Reverse Order Of Rows / Columns	Select Using Control Register
Temperature Sensor	0.75 V ± 0.05 V @ 300 K 1.07 V ± 0.05 V @ 77 K	Temp Pad
Full Frame Rate (Pixel Rate 22.2 MHz and T = 77 K)	8 Output ≥ 30 FPS 16 Output ≥ 60 FPS	37 FPS (Binning mode: 131 FPS) 66 FPS (Binning mode: 215 FPS)
Data Valid / Settling Time	Settle to 0.1% @ T=77 K in ≤ 35 ns	12 pF // 100 kΩ load Default power settings
Adjacent ROIC Pixel Crosstalk	< 0.05% @ T=77 K < 0.5% @ T=300 K	
Non-Adjacent Multiplexing ROIC Pixel Crosstalk	< 0.05% @ T=77 K < 0.5% @ T=300 K	
Frame-Frame ROIC Pixel Crosstalk	< 0.5% @ T=77 K < 0.5% @ T=300 K	
Minimum Window Size and Resolution	64 (centered) columns x 8 rows 128 (centered) columns x 8 rows	8 Output Mode 16 Output Mode
Die Size	24 mm x 25.5 mm	