

FLIR ISC0403

Standard 640x512 ROIC (15umx15um Pixel)

Version 100 – initial release Nov. 2004 for version 100 of the ROIC design

Version 200 – updated release per version 200 of the ROIC design – July 2005

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(15umx15um Pixel)

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ROIC PARAMETER	SPECIFICATION REQUIREMENT	COMMENTS
Array Configuration	640 x 512	
Pixel Size in Columns	15um	
Detector Impedance	$> 10 \times 10^3$ (Ohm.cm ²)	Used for Simulation
Detector Capacitance	≤ 0.1 pF	Used for Simulation
Crosstalk	< 20%	
Signal Loss due to Fill Factor	< 5%	
Hybridization	Indium Bump	

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ISC0403 Specification and Requirements Review (1 of 6)

ROIC PARAMETER	SPECIFICATION REQUIREMENT	COMMENTS
Array Configuration	640 x 512	
Pixel Pitch in Columns	15um	
Pixel Pitch in Rows	15um	
Input Polarity	P-on-N	(Current Flows into Inputs) InSb, InGaAs, HCT
Input Configuration	Direct Injection (DI)	
Core Multiplexing Configuration	Voltage Mode	
Detector Impedance	$\geq 10 \times 10^3$ (Ohm.cm ²)	Used for Simulation
Detector Capacitance	≤ 0.1 pF	Used for Simulation
Temperature of Operation	80K (Liquid Nitrogen Temperature)	All specification specified for 80K. Room temperature operation will have reduced performance

ISC0403 Specification and Requirements Review (2 of 6)

ROIC PARAMETER	SPECIFICATION REQUIREMENT	COMMENTS
Input Biases	VPOS 3.6V	Analog Positive Output
	VPOSOUT 3.6V	Positive Supply
	VPOSD 3.6V	Digital Positive for level shifter
	VPD 3.6V	Digital Positive Note: VPD Voltage Should = VPOSOUT Voltage
	VNEG 0.0V	Analog Negative
	VNEGOUT 0.0V	Output Neg Supply
	VND 0.0V	Digital Negative
	VREF 1V	Analog Reference VREF <input type="checkbox"/> V (Option: Internal or external reference) → 7 feedthroughs + 1 optional (VREF)
Input Clocks	<u>Name</u> <u>Vhigh to Vlow</u>	
	CLK VPD to VND	Master Clock
	LSYNC VPD to VND	Line Sync
	FSYNC VPD to VND	Frame Sync (Integ. Control)
	DATA VPD to VND	Mode Control
	RESET_B VPD to VND	Master Reset (optional) → 4 feedthroughs + 1 optional (RESET_B)
Input Clock	10% to 90% in 10nS	
Outputs	Selectable 1, 2 or 4 with Reference Output	Default = 1 outputs → 4 feedthroughs + 1 optional reference

- **Minimum of 15 feedthroughs (4 outputs) + 3 optional VREF, RESET_B, OUTR**
- **Minimum of 12 feedthroughs (1 output) + 3 optional VREF, RESET_B, OUTR**

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ROIC PARAMETER	SPECIFICATION REQUIREMENT	COMMENTS
Power	No reference output @ Max Tint @ Min Tint ≤ 35 mW ≤ 45 mW 1 Output ≤ 45 mW ≤ 54 mW 2 Outputs ≤ 62 mW ≤ 71 mW 4 Outputs	Estimated Values @ Max Tint @ Min Tint 32mW est 41mW est 41mW est 50mW est 57mW est 66mW est
	With 6 reference columns + one reference output @ Max Tint @ Min Tint ≤41 mW ≤ 50 mW 1 Output ≤ 50 mW ≤ 59 mW 2 Outputs ≤ 67 mW ≤ 77 mW 4 Outputs	Estimated Values @ Max Tint @ Min Tint 37mW est 46mW est 46mW est 55mW est 62mW est 71mW est
Control Register Functions	Programmable Test I/O Anti-blooming control Power Control Master Current Detector Bias Adj. Invert/Revert Windowing (programmable size and position) 1, 2 or 4 Outputs Integration Mode (ITR, IWR, NDRO) Reference Output Enable Global Reset	Default = 1 outputs

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Programmable Test	Test Row Input Unit Cell Test Injection VET Circuit	
Detector Bias Adjust	-100mV to 500mV Adjustment @ nominal current (1nA)	7 bit bias control

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ROIC PARAMETER	SPECIFICATION REQUIREMENT	COMMENTS
Input Current	From 10pA to 0.5nA	Used for simulations Depends on f number and background temperature
Input Charge Handling	$\geq 6.5 \times 10^6$ carriers	$C_{INT} + C_{SH} = 0.578 \text{pF at } 2\text{V} \rightarrow 7.20 \times 10^6 \text{ carriers}$
Non- Linearity	$< \pm 0.5\%$ from least squares line fit	Output Voltage vs. Tint Max Dev. from least squares fit over 10% to 80% of full range (unique range for each power setting)
Output Interface	$\geq 100\text{k Ohms}$ $\leq 15\text{pF external capacitance}$	25pF total load capacitance, including bond pad, bonding wire
Output Voltage Swing	$2.0\text{V} \pm 0.2\text{V}$ (Baseline $\approx 1.0\text{V} \pm 0.1\text{V}$)	With Defaults: $\approx 1.8\text{V} \pm 0.2\text{V}$ Typical Output Range at 300k $\approx 2\text{V} \pm 0.2\text{V}$ Typical Output Range at 80K
Noise	Output Noise 200uV Input referred noise 715 e ⁻ _{RMS} Signal-to-Noise Ratio 80dB	Spec values are theoretical plus 10% Without Detector or System Noise

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ROIC PARAMETER	SPECIFICATION REQUIREMENT	COMMENTS
<p>Column Output Order 1 Output Mode Output A</p> <p>2 Output Mode Output A Output B</p>	<p>Column 0,1,...,639</p> <p>Column 0,2,...,638 Column 1,3,...,639</p>	<p>One Output Mode Normal Readout Direction</p> <p>Two Output Mode Normal Readout Direction</p>
<p>4 Output Mode Output A Output B Output C Output D</p>	<p>Column 0,4,...,636 Column 1,5,...,637 Column 2,6,...,638 Column 3,7,...,639</p>	<p>Four Output Mode Normal Readout Direction</p>
<p>Invert / Revert</p>	<p>Reverse Order of Rows and/or Columns</p>	<p>Select using Control Register</p>
<p>Temperature Sensor</p>	<p>0.75V ± 0.05V @ 300K 1.05V ± 0.05V at 77K</p>	<p>Test/Temp Pad Measured values on ISC0403_V1 → 1 additional feedthrough</p>

ISC0403 Specification and Requirements Review (6 of 6)

ROIC PARAMETER	SPECIFICATION REQUIREMENT	COMMENTS
Full Frame Rate Pixel Rate 12MHz	1 Output ≥ 30 FPS 2 Output ≥ 60 FPS 4 Output ≥ 120 FPS	CLK rate = 6MHz Output rate = 12MHz
Data Valid / Settling Time	Settle to 0.1% @ T=80K in ≤ 55ns Settle to 0.8% @ T=300K in ≤ 55ns	External load capacitance 15pF // 100kΩ pad As simulated at room temp.
Adjacent Pixel Crosstalk (ROIC)	< 0.1% @ T=80K < 0.8% @ T=300K	
Non-Adjacent Pixel Crosstalk (ROIC)	< 0.1% @ T=80K < 0.8% @ T=300K	
Minimum Window Size (Max Frame Rate)	4 columns x 4 Rows 8 columns x 4 Rows 16 columns x 4 Rows	1 Output Mode (4.16kF/s) 2 Output Mode (4.16kF/s) 4 Output Mode (4.16kF/s)
Die Size	12.5 mm x 11.43 mm	Layout dimension (to scribe line edge) NOT physical die size Optical center offset Δx=0, Δy=+435um