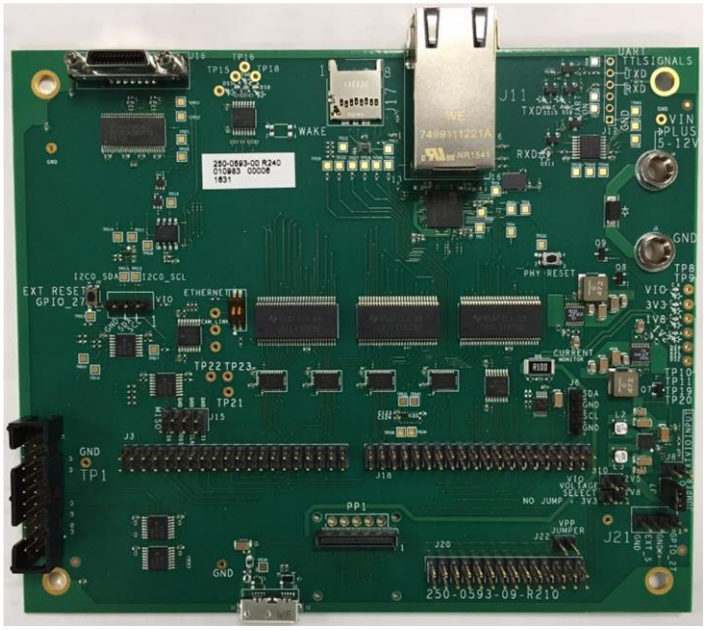
FLIR Boson Development Board

Official Publication Date: 12/18/2018
Official Expiration Date: Until Next Release



FLIR Boson Development Board

Revision History

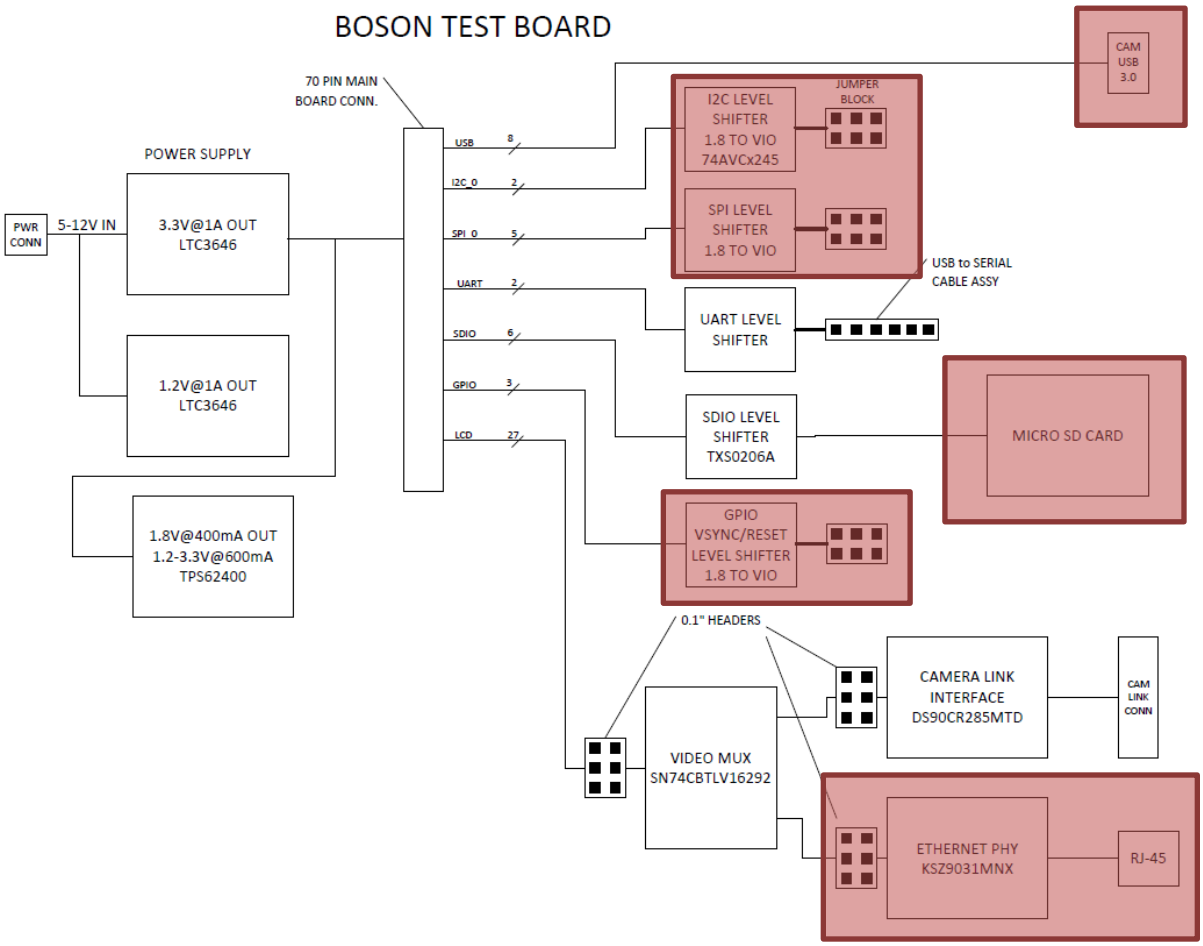
Version	Date	Comments
100	12/06/2016	Initial Release
111	6/20/2017	Updated Formatting
112	5/24/2018	Added notes about unreleased features, Removed <9Hz from title
113	12/18/2018	Updated footer for export statement Added information regarding “cmos_data_valid” signal not available on current revision of development board

Scope

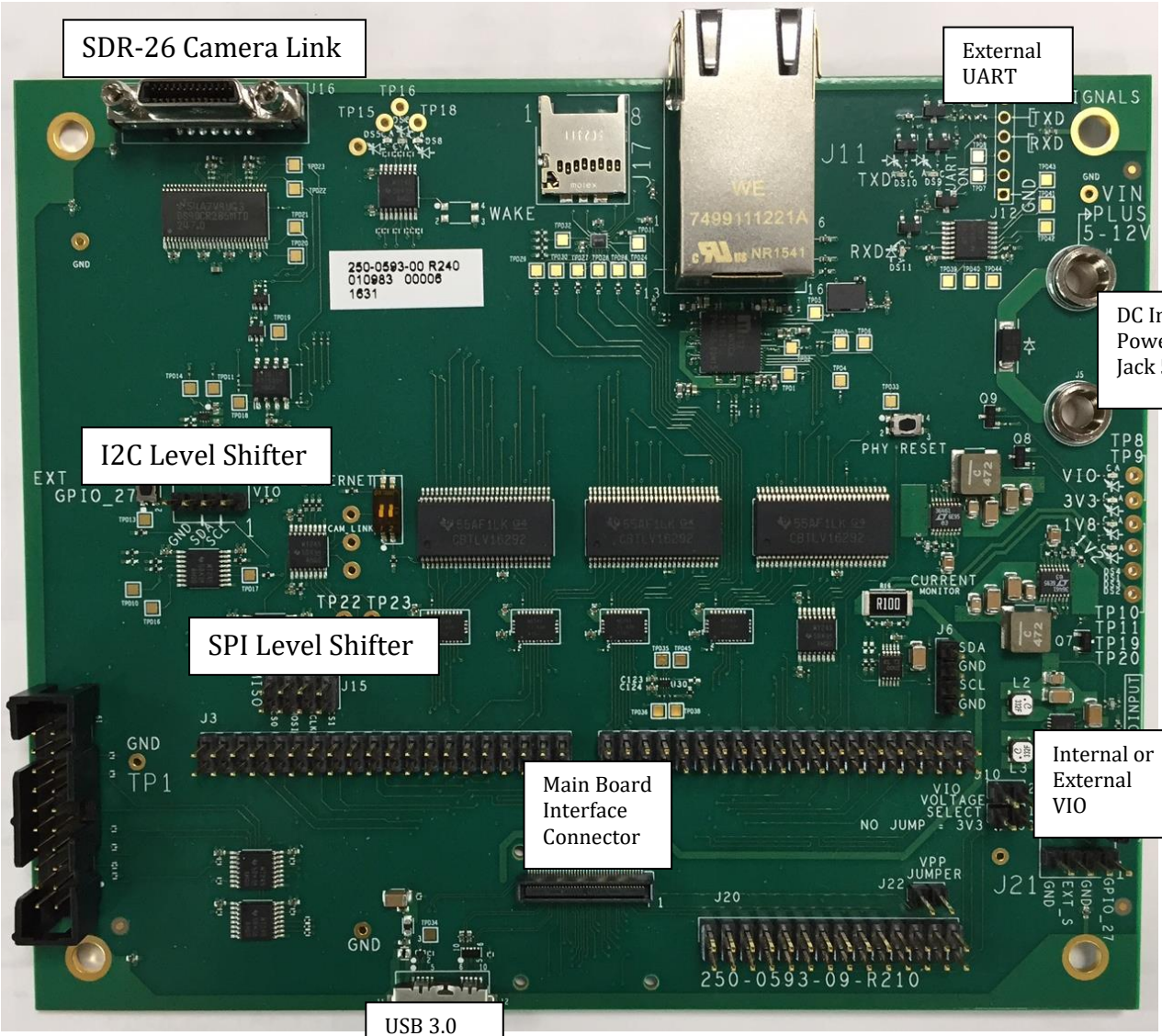
This note is intended to provide a better understanding of the Boson Development board and how to use it to connect to the various SW interfaces available to Boson. For details regarding the SW interface, please refer to the Datasheet (Ref 1) and Software IDD (Ref 2). Please note: many modules listed in this guide are not currently implemented in Boson code, and many will not be implemented in the near term.

Block Diagram Overview

The below Block Diagram shows all of the interfaces available on the development PCB. Please note that not all interfaces are implemented in the Boson software. Interfaces that have not been implemented are marked below in red and please refer to the datasheet for the updated Boson interface specification. The 80 Pin Main Board Connector can be interfaced with directly by using the header pins J3 and J18. Alternatively, the Boson Test Board has alternate interfaces shown below:



FLIR Boson Development Board

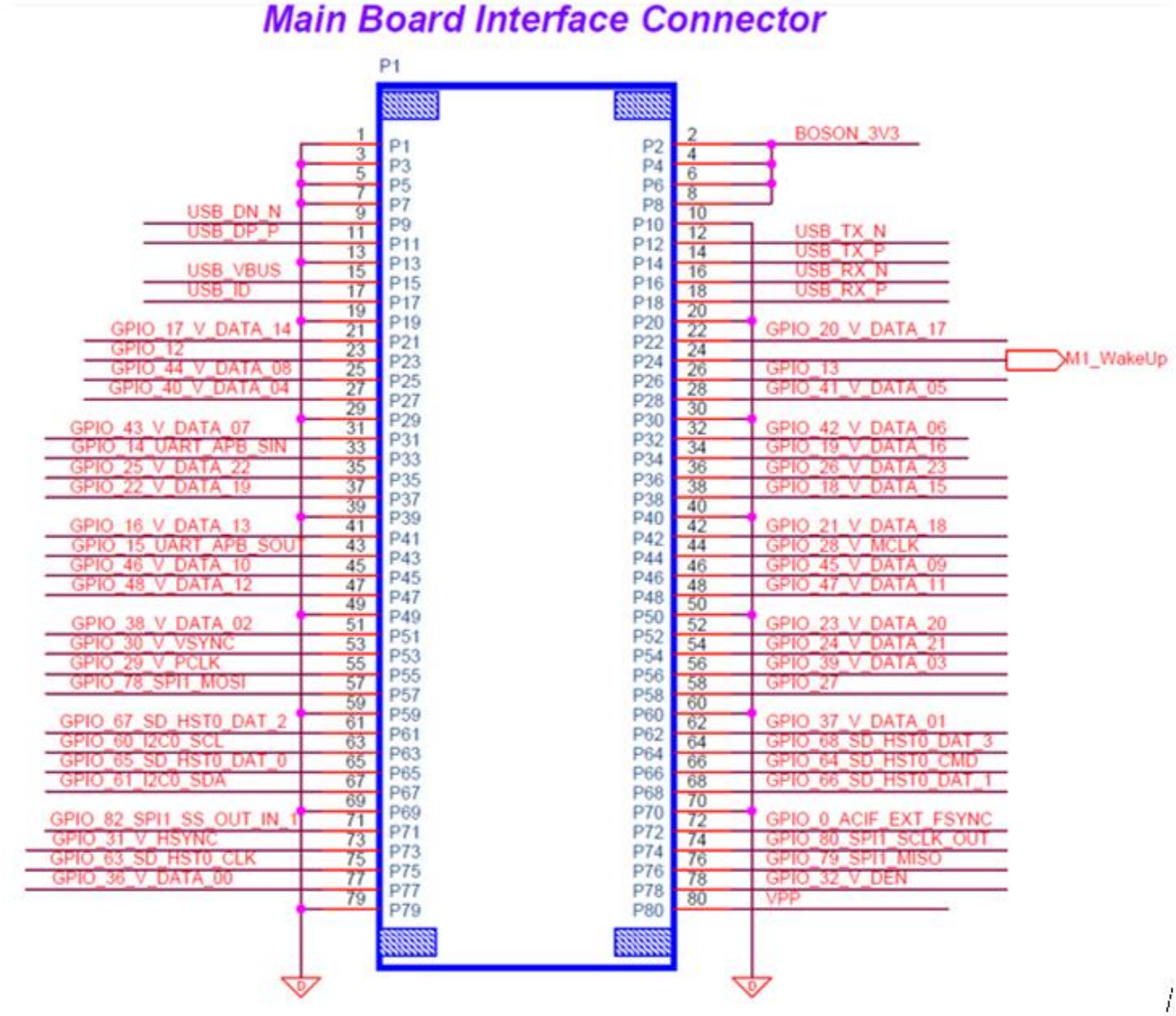


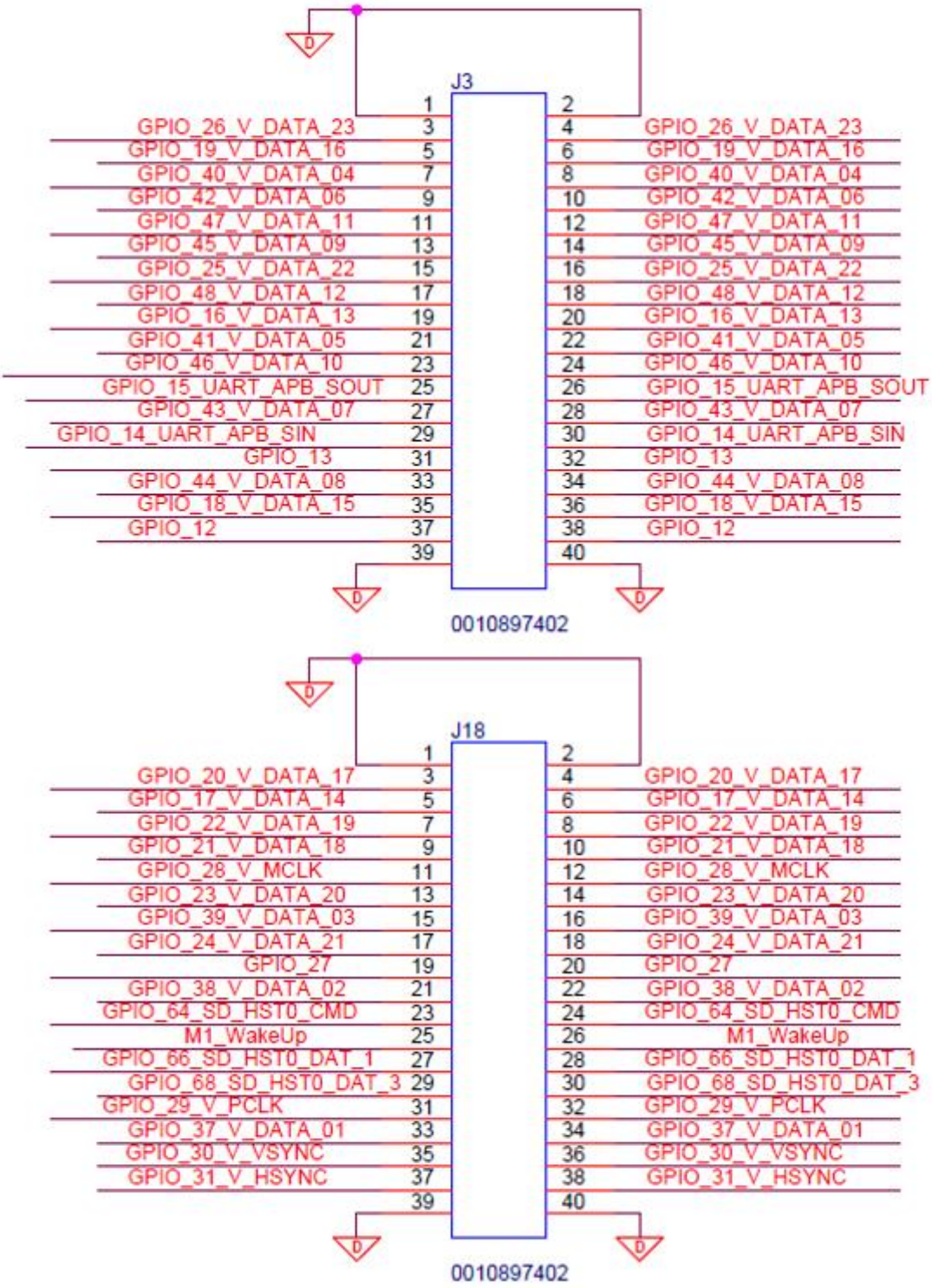
Pinout Description

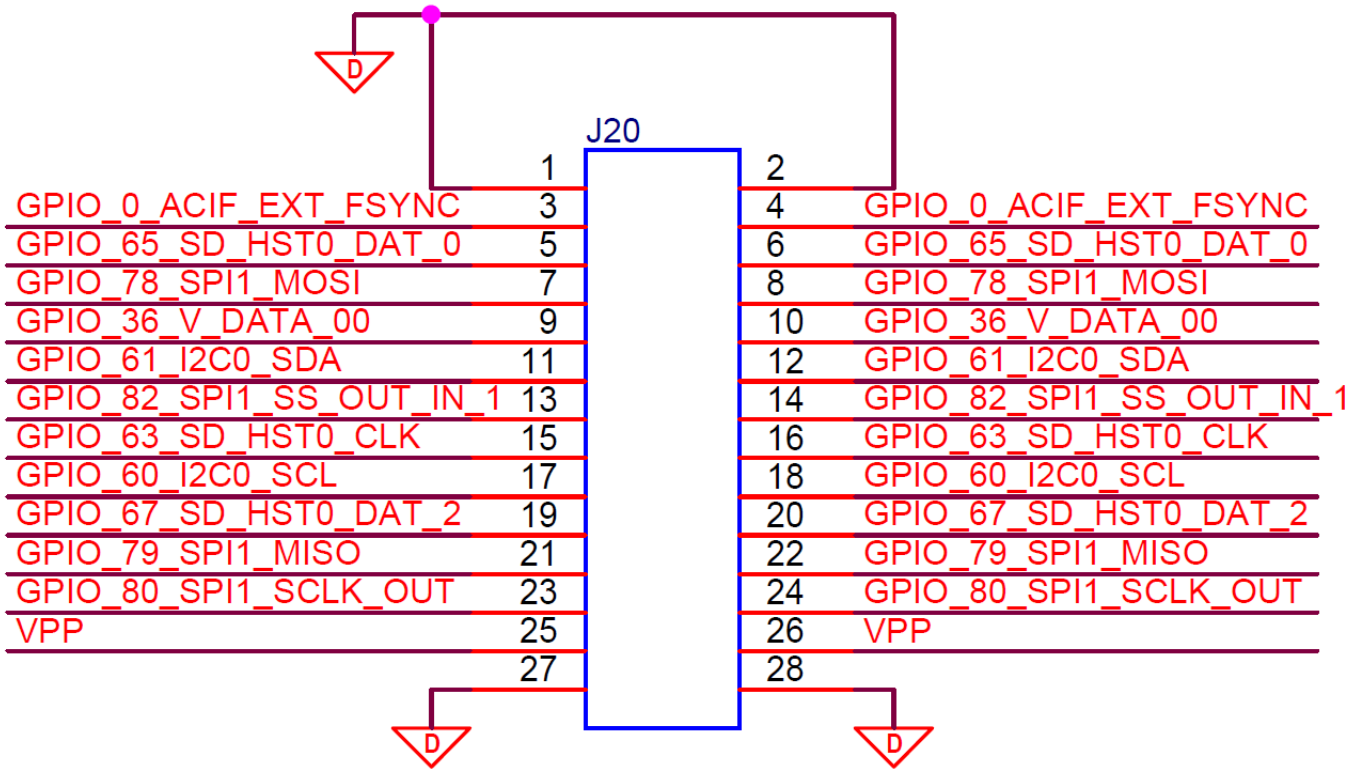
The Following sections briefly describe each module and provide a pinout diagram.

Main Board Interface Connector

The Header connectors J3, J18, and J20 connect directly to the Boson's 80 Pin Main Board Interface. For the pinout definition on the Boson, please refer to the Datasheet for more details. **Please Note:** Pin 78, "cmos_data_valid" is not routed to the header connectors on the current revision of Boson development board. The pinout between headers J3, J18, J20 and Main connector P1:







DC Input Power

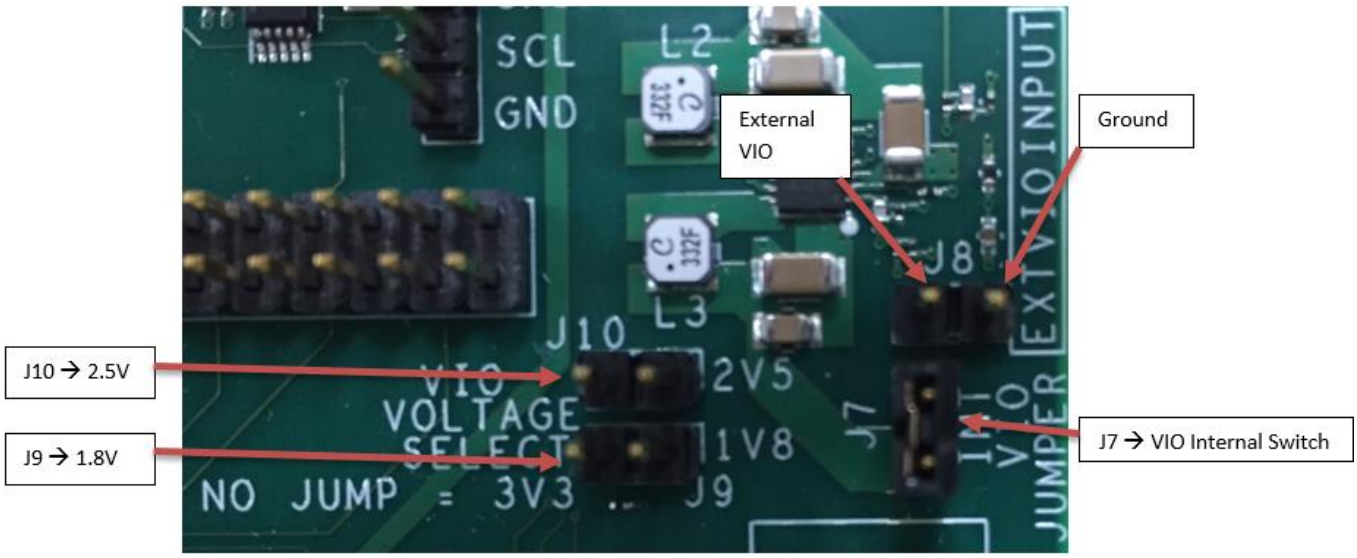
The Banana plug inputs for DC power take 5-12 Volts of input voltage. This drives a 3.3V power supply for the Boson's input power. Additionally, the DC power input drives an internal IO Voltage (VIO) power supply used for the I2C and SPI level shifter.

IO Voltage

The IO voltage used in the SPI and I2C Level shifters can be driven by the Dev Board power supply by connecting across the J7 jumper. If the VIO is supplied by the dev board power supply, then connecting across the following jumpers will yield the following IO Voltage:

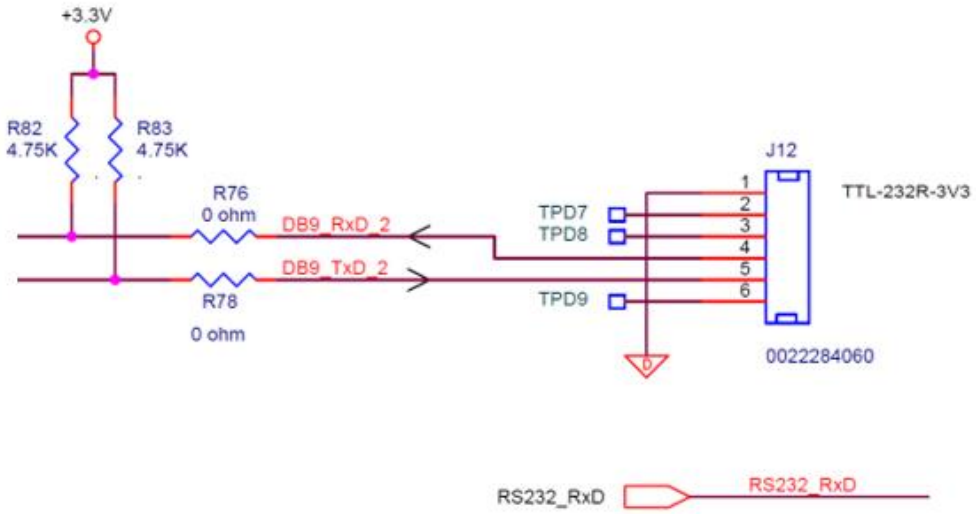
J9	→ 1.8 Volts
J10	→ 2.5 Volts
Neither	→ 3.3 Volts

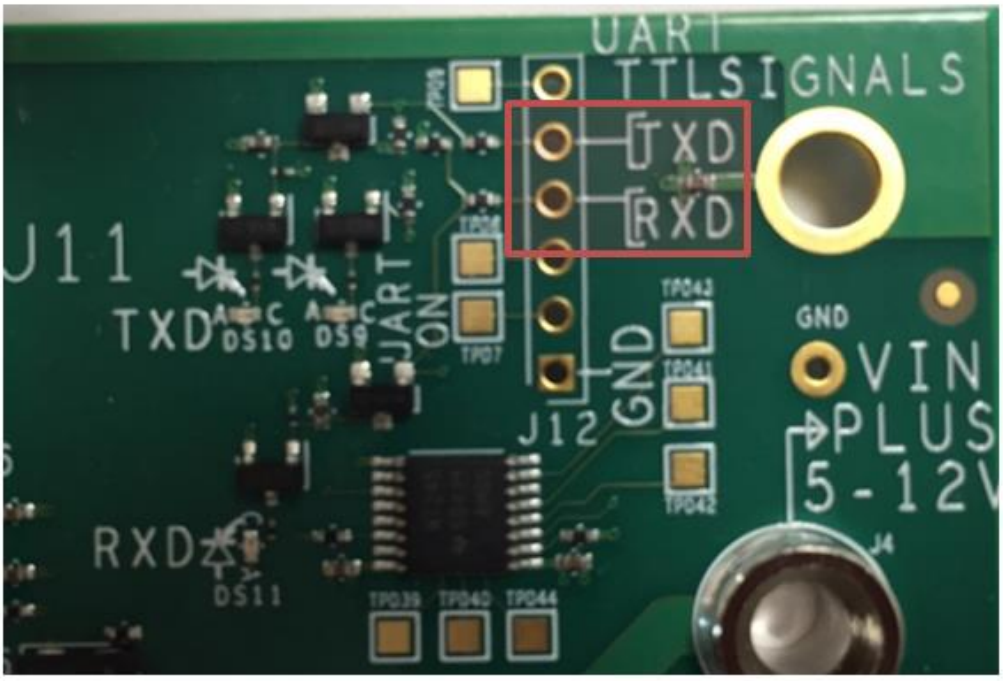
If a user desires to set VIO by an external power supply, then jumper J7 should be disconnected and the external IO voltage should be applied across J8. Note: External VIO input must be greater than 1.8V



External UART

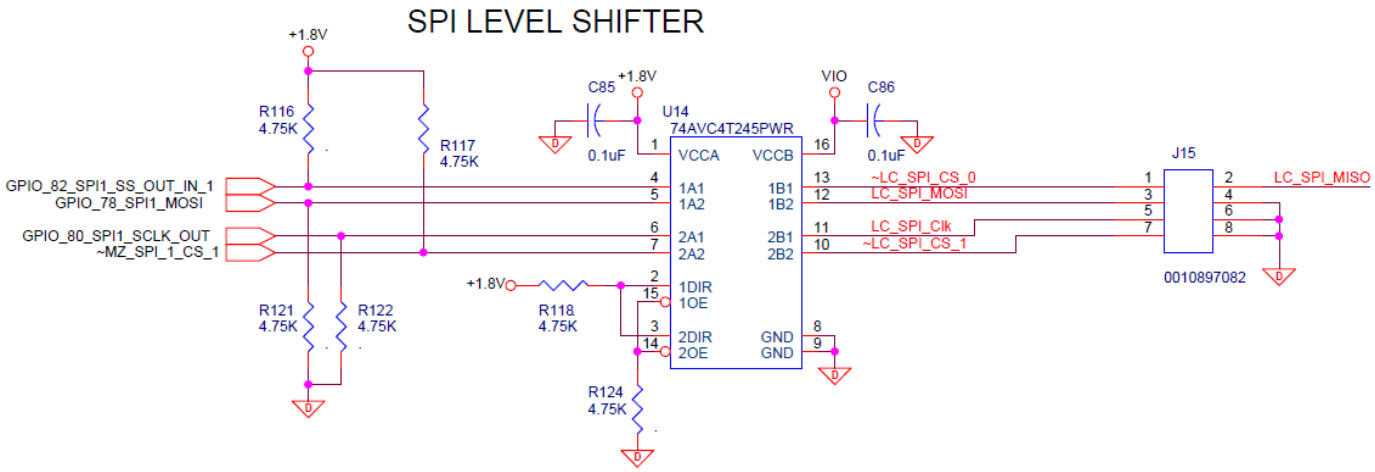
The external UART interface takes 3.3V serial communication. This signal is level shifted down to 1.8V to be sent to the boson. Additionally, a signal mux is available to switch the Boson UART input between the External UART and the Ethernet PHY. By default the mux is set to the External UART. Additionally, Ethernet support is currently not available on Boson. The schematic For J12 is shown below:

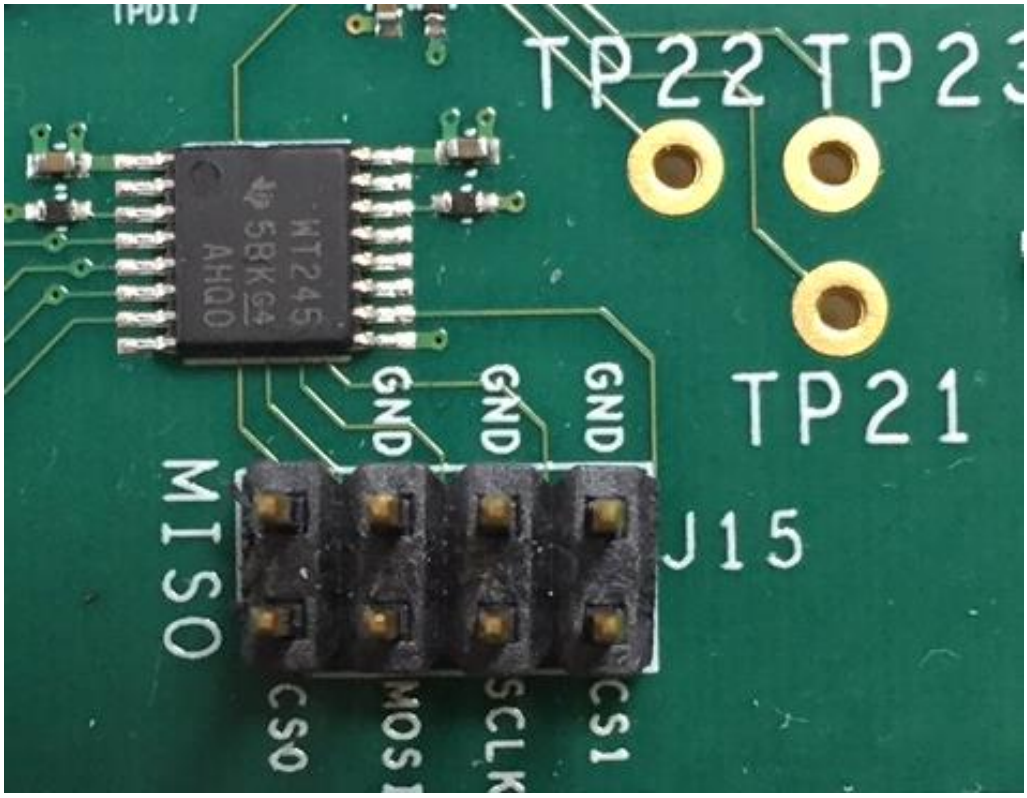




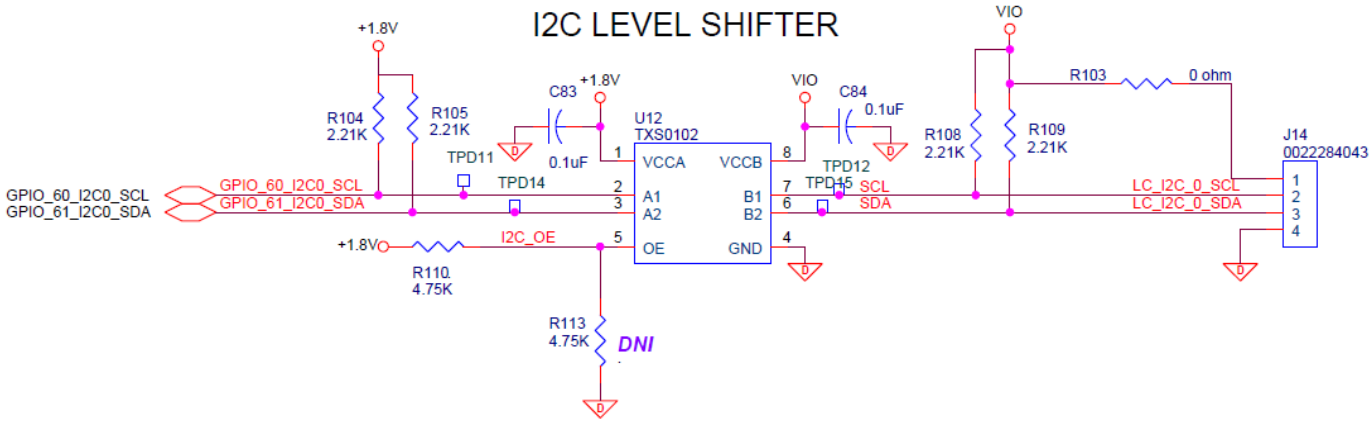
SPI Level Shifter (Will not be implemented in the near term)

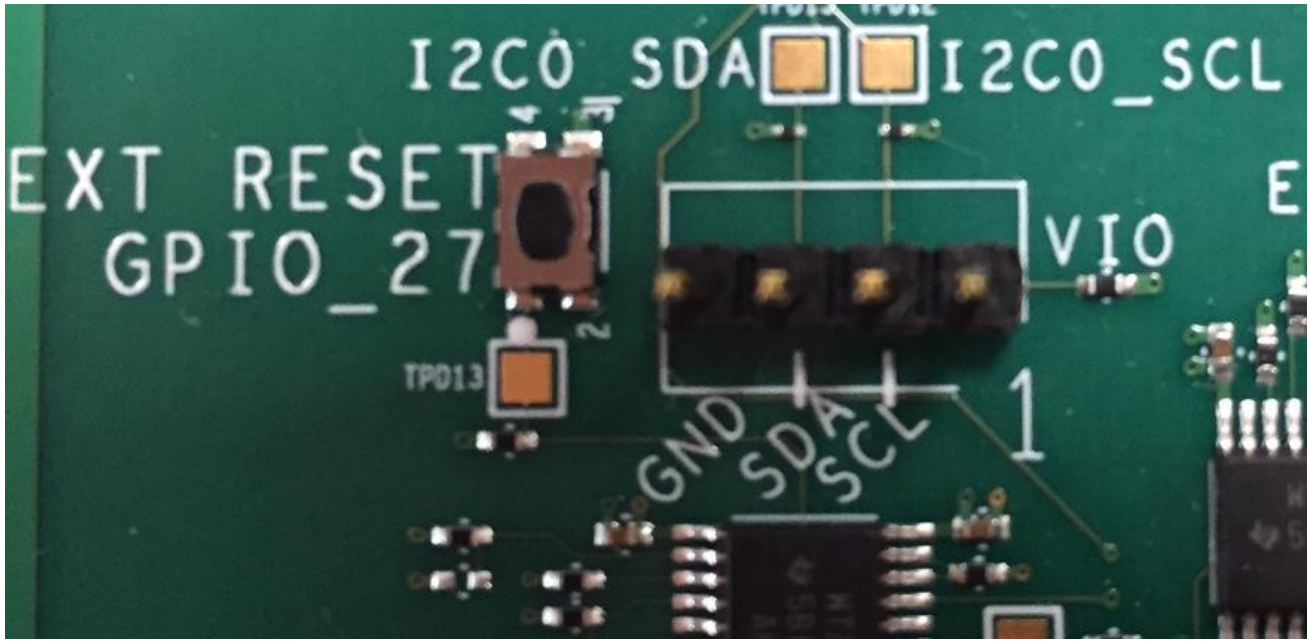
The input voltage of the SPI interface is defined by The IO Voltage described in section 3.3. This input voltage is level shifted down to the appropriate 1.8 volts specified by the Boson GPIO input. The schematic for J15 is shown below:





I2C Level Shifter (Will not be implemented in the near term)
Similar to the SPI Level shifter, the input voltage of the I2C interface is defined by the IO Voltage described in section 3.3. This input voltage is level shifted down to the appropriate 1.8 bolts specified by the Boson GPIO input. The schematic for J14 is shown below:





Ethernet (Will not be implemented in the near term)
Currently Not Implemented

SD Card Interface (Will not be implemented in the near term)
Currently not implemented